WHAT IS CLAIMED IS:

1. An input and output (I/O) circuit comprising:

an output buffer having an NMOS transistor coupled to a PMOS transistor;

an ESD protection circuit having a parasitic silicon controlled rectifier (SCR) integrated therein, and coupled to the output buffer; and

a diode string having a predetermined number of diodes coupled between a source node of the NMOS transistor and ground,

wherein a voltage drop across the diode string increases the SCR holding voltage, thereby setting an ESD protection holding voltage for the ESD protection circuit.

2. The circuit of claim 1 wherein the number of the diodes in the diode string is determined by a positive supply voltage and the SCR holding voltage.

3. The circuit of claim 1 wherein the NMOS transistor is realized by using two asymmetric NMOS transistors.

4. The circuit of claim 1 wherein the NMOS transistor is realized by using a transistor layout for enhancing a turn-on speed of the ESD protection circuit.

5. The circuit of claim 1 wherein the SCR has an increased beta-gain product of two transistors therein.

6. The circuit of claim 1 wherein the diode string has two or fewer diodes for a positive supply voltage of about 2.5V or less.

7. The circuit of claim 1 wherein the diode string has four, or fewer diodes, for a positive supply voltage of about 3.3V or less.

8. An input and output (I/O) circuit comprising:

an output buffer having an NMOS transistor coupled to a PMOS transistor;

an ESD protection circuit having a parasitic silicon controlled rectifier (SCR) integrated therein and coupled to the output buffer; and

a diode string having four, or fewer diodes, coupled between a source node of the NMOS transistor and ground,

wherein a voltage drop across the diode string increases the SCR holding voltage, thereby setting an ESD protection holding voltage for the ESD protection circuit.

9. The circuit of claim 8 wherein the number of the diodes in the diode string is determined by a positive supply voltage and the SCR gate holding voltage.

10. The circuit of claim 8 wherein the NMOS transistor is realized by using two asymmetric NMOS transistors.

11. The circuit of claim 8 wherein the NMOS transistor is realized by using a transistor layout for enhancing a turn-on speed of the ESD protection circuit.

12. The circuit of claim 8 wherein the SCR has an increased beta-gain product of two transistors therein.

13. A layout for an output buffer having an NMOS transistor comprising:

a N well region having a P+ region contained therein; and

two asymmetrical NMOS transistors formed on two sides of the P+ region;

wherein a portion of the P+ region in the N well region provides at least one resistor for a parasitic silicon controlled rectifier (SCR), and

wherein a diode string having a predetermined number of diodes is coupled between a source node of the NMOS transistors and ground.

14. The layout of claim 13 wherein the number of the diodes in the diode string is determined by a positive supply voltage and the SCR gate holding voltage.

15. The layout of claim 13 wherein the SCR has an increased beta-gain product of two transistors therein.

16. The layout of claim 13 wherein the diode string has two or fewer diodes for a positive supply voltage of about 2.5V or less.

17. The layout of claim 13 wherein the diode string has four, or fewer diodes, for a positive supply voltage of about 3.3V or less.

18. The layout of claim 13 further comprising one or more guard rings for collecting minority carriers.

19. The layout of claim 13 wherein a center portion of the P+ region is connected to an input/output pad.